PCT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION**	see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.
SC0704EM/PCT		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/EP 99/ 04291	21/06/1999	27/06/1998
Applicant		
MOTOROLA GMBH et al.		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 3 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language,** the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   [ ] the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

   b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :

   [ ] contained in the international application in written form.

   [ ] filed together with the international application in computer readable form.

   [ ] furnished subsequently to this Authority in written form.

   [ ] furnished subsequently to this Authority in computer readble form.

   [ ] the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

   [ ] the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. [ ] **Certain claims were found unsearchable** (See Box I).

3. [ ] **Unity of invention is lacking** (see Box II).

4. With regard to the **title,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is Figure No. 1

   [X] as suggested by the applicant.

   [ ] because the applicant failed to suggest a figure.

   [ ] because this figure better characterizes the invention.

   [ ] None of the figures.

WO 00/01060
PCT/EP99/04291

PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

To:
IBBOTSON, Harry
Motorola European Intellectual
Property Operations
Midpoint, Alencon Link
Basingstoke
Hampshire RG21 7PL
ROYAUME-UNI

NOTICE INFORMING THE APPLICANT OF THE COMMUNICATION OF THE INTERNATIONAL APPLICATION TO THE DESIGNATED OFFICES

(PCT Rule 47.1(c), first sentence)

Date of mailing (day/month/year)	
06 January 2000 (06.01.00)	
Applicant's or agent's file reference	**IMPORTANT NOTICE**
SC0704EM/PCT	

International application No.	International filing date (day/month/year)	Priority date (day/month/year)
PCT/EP99/04291	21 June 1999 (21.06.99)	27 June 1998 (27.06.98)

Applicant MOTOROLA GMBH et al

1. Notice is hereby given that the International Bureau has communicated, as provided in Article 20, the international application to the following designated Offices on the date indicated above as the date of mailing of this Notice:
EP,US

In accordance with Rule 47.1(c), third sentence, those Offices will accept the present Notice as conclusive evidence that the communication of the international application has duly taken place on the date of mailing indicated above and no copy of the international application is required to be furnished by the applicant to the designated Office(s).

2. The following designated Offices have waived the requirement for such a communication at this time:
None

The communication will be made to those Offices only upon their request. Furthermore, those Offices do not require the applicant to furnish a copy of the international application (Rule 49.1(a-bis)).

3. Enclosed with this Notice is a copy of the international application as published by the International Bureau on 06 January 2000 (06.01.00) under No. WO 00/01060

REMINDER REGARDING CHAPTER II (Article 31(2)(a) and Rule 54.2)

If the applicant wishes to postpone entry into the national phase until 30 months (or later in some Offices) from the priority date, a demand for international preliminary examination must be filed with the competent International Preliminary Examining Authority before the expiration of 19 months from the priority date.

It is the applicant's sole responsibility to monitor the 19-month time limit.

Note that only an applicant who is a national or resident of a PCT Contracting State which is bound by Chapter II has the right to file a demand for international preliminary examination.

REMINDER REGARDING ENTRY INTO THE NATIONAL PHASE (Article 22 or 39(1))

If the applicant wishes to proceed with the international application in the national phase, he must, within 20 months or 30 months, or later in some Offices, perform the acts referred to therein before each designated or elected Office.

For further important information on the time limits and acts to be performed for entering the national phase, see the Annex to Form PCT/IB/301 (Notification of Receipt of Record Copy) and Volume II of the PCT Applicant's Guide.

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. (41-22) 740.14.35

Authorized officer
J. Zahra

Telephone No. (41-22) 338.83.38

PCT
WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H02M 7/00, H01L 25/16

A1

(11) International Publication Number: WO 00/01060

(43) International Publication Date: 6 January 2000 (06.01.00)

(21) International Application Number: PCT/EP99/04291

(22) International Filing Date: 21 June 1999 (21.06.99)

(30) Priority Data:
9813888.6 27 June 1998 (27.06.98) GB

(71) Applicant *(for all designated States except US)*: MOTOROLA GMBH [DE/DE]; Heinrich–Hertze–Strasse 1, D–6204 Taunusstein 4 (DE).

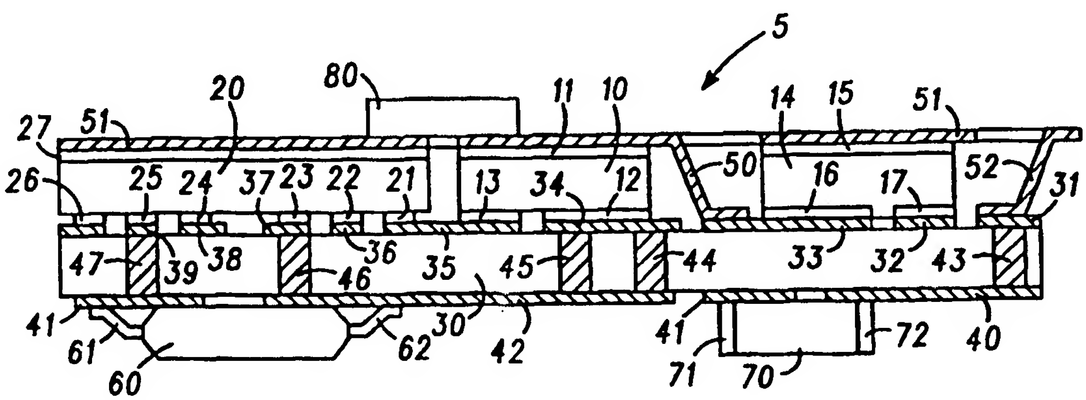
(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: TRIANTAFYLLOU, Markos [GR/DE]; Krausstrasse 3, D–81929 Munich (DE). SPECKS, Will [DE/DE]; Flensburger, Sur. 67, D–81929 Munich (DE). ESCOFFRE, Claude [FR/DE]; Hagenauer Strasse 8b, D–81479 Munich (DE).

(74) Agents: IBBOTSON, Harry et al.; Motorola European Intellectual Property Operations, Midpoint, Alencon Link, Basingstoke, Hampshire RG21 7PL (GB).

(81) Designated States: US, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: ELECTRONIC PACKAGE ASSEMBLY



(57) Abstract

An electronic package assembly includes a number of semiconductor devices with first and second sides. A printed circuit substrate has a number of printed circuit patterns bonded to conductive pads of the first sides of the devices. A metal leadframe includes leads which provide external connections for the package assembly, and also includes a non–lead island portion bonded to conductive pads of the second sides of the devices. In this way the island portion of the leadframe forms an interconnection between the second sides of the devices.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania
AM	Armenia
AT	Austria
AU	Australia
AZ	Azerbaijan
BA	Bosnia and Herzegovina
BB	Barbados
BE	Belgium
BF	Burkina Faso
BG	Bulgaria
BJ	Benin
BR	Brazil
BY	Belarus
CA	Canada
CF	Central African Republic
CG	Congo
CH	Switzerland
CI	Côte d'Ivoire
CM	Cameroon
CN	China
CU	Cuba
CZ	Czech Republic
DE	Germany
DK	Denmark
EE	Estonia
ES	Spain
FI	Finland
FR	France
GA	Gabon
GB	United Kingdom
GE	Georgia
GH	Ghana
GN	Guinea
GR	Greece
HU	Hungary
IE	Ireland
IL	Israel
IS	Iceland
IT	Italy
JP	Japan
KE	Kenya
KG	Kyrgyzstan
KP	Democratic People's Republic of Korea
KR	Republic of Korea
KZ	Kazakstan
LC	Saint Lucia
LI	Liechtenstein
LK	Sri Lanka
LR	Liberia
LS	Lesotho
LT	Lithuania
LU	Luxembourg
LV	Latvia
MC	Monaco
MD	Republic of Moldova
MG	Madagascar
MK	The former Yugoslav Republic of Macedonia
ML	Mali
MN	Mongolia
MR	Mauritania
MW	Malawi
MX	Mexico
NE	Niger
NL	Netherlands
NO	Norway
NZ	New Zealand
PL	Poland
PT	Portugal
RO	Romania
RU	Russian Federation
SD	Sudan
SE	Sweden
SG	Singapore
SI	Slovenia
SK	Slovakia
SN	Senegal
SZ	Swaziland
TD	Chad
TG	Togo
TJ	Tajikistan
TM	Turkmenistan
TR	Turkey
TT	Trinidad and Tobago
UA	Ukraine
UG	Uganda
US	United States of America
UZ	Uzbekistan
VN	Viet Nam
YU	Yugoslavia
ZW	Zimbabwe

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H02M7/00 H01L25/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H02M H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	DE 35 31 235 A (VEB KOMBINAT ROBOTRON) 3 April 1986 (1986-04-03) abstract page 10, line 34 -page 11, line 23 figures 2-5	1
A	US 5 532 512 A (RAYMOND A.FILLION ET AL.) 2 July 1996 (1996-07-02) abstract figures 6,8	1
A	DE 196 03 224 A (WOLFGANG SCHUSTER) 31 July 1997 (1997-07-31) abstract column 3, line 18 - line 28	1

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 October 1999	21/10/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Lund, M

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP 99/04291

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4 965 710 A (BRIAN R.PELLY ET AL.) 23 October 1990 (1990-10-23) abstract figure 5 column 5, line 64 -column 6, line 34	1

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
DE 3531235 A	03-04-1986	DD 231169 A	18-12-1985
		DD 231172 A	18-12-1985
		DD 228940 A	23-10-1985
		DD 230112 A	20-11-1985
		DD 231170 A	18-12-1985
		DD 231171 A	18-12-1985
		DD 231168 A	18-12-1985
US 5532512 A	02-07-1996	NONE	
DE 19603224 A	31-07-1997	NONE	
US 4965710 A	23-10-1990	DE 4036426 A	29-05-1991
		DE 9018172 U	13-11-1997
		GB 2238167 A,B	22-05-1991
		IT 1243869 B	28-06-1994
		JP 10144863 A	29-05-1998
		JP 3209756 A	12-09-1991
		JP 8028464 B	21-03-1996

ELECTRONIC PACKAGE ASSEMBLY

Field of the Invention

This invention relates to an electronic package assembly and preferably but not exclusively to an electronic package assembly incorporating a power transistor.

Background of the Invention

In many electronic applications, particularly in automotive applications, power and logic devices are used in conjunction with each other, to perform a single function.

For example, an electric motor for operating an automatic sunroof or a window of a vehicle is typically actuated by a high-sided switch formed by power transistors. In order to reduce power consumption, the high-sided switch is ideally placed as close as possible to the electric motor, thus keeping the length of high current paths to a minimum and hence reducing unnecessary power losses.

Typically the driver of a vehicle may prefer to operate a separate switch on the dashboard of the vehicle, which then sends a (low-power) signal to the high-sided switch, in order to actuate it. Therefore a certain amount of logic circuitry is required, preferably at the high-sided switch, in order to control the actuation and other ancillary functions, such as fail-safe features.

Therefore there is a need to incorporate logic integrated circuits and power transistors into a single package module, which is ideally adapted to be mounted on or in close proximity to the electric motor.

A problem with existing combined logic/power packages is that the high power requirements of the high-sided switch do not easily facilitate integration with low power logic integrated circuits. The high currents involved preclude the use of conventional wire bond techniques, and the thermal management of heat dissipation presents further problems.

This invention seeks to provide an electronic package assembly which mitigates the above mentioned disadvantages.

Summary of the Invention

According to the present invention there is provided an electronic package assembly comprising: a plurality of semiconductor devices, each having a first side with a plurality of conductive pads, at least two of the plurality of devices being vertical power transistor devices having a second side opposite the first side, the second side having further conductive pads; a printed circuit substrate, having a plurality of printed circuit patterns bonded to the conductive pads of the first sides of the plurality of semiconductor devices, and arranged to provide logic interconnections between the plurality of semiconductor devices; and, a leadframe including leads which provide external connections for the package assembly, and having a non-lead island portion bonded to the further conductive pads of the second sides of the at least two vertical power transistor devices, wherein the island portion of the leadframe forms a power interconnection between the at least two vertical power transistor devices.

Preferably the leadframe further comprises a substrate lead portion, which is arranged to connect to a further pad of the printed circuit substrate, thereby directly connecting the leadframe to the substrate. The substrate lead portion is preferably connected to the island portion of the leadframe such that the conductive pads of the second sides of the semiconductor devices are directly electrically connected to the substrate.

Preferably a discrete electronic device is mounted directly onto the leadframe. The leadframe preferably has contact bumps to which the electronic device is coupled.

The semiconductor device may be a vertical H-bridge power transistor device. Alternatively, the semiconductor device may be a full-bridge high-sided switch arrangement.

The substrate preferably has a first face having the plurality of pads, and a second face opposite the first face to which further electronic devices are attached. Preferably the substrate is provided with electrical vias arranged to electrically interconnect the first and the second faces of the substrate. Preferably the substrate is also provided with thermal vias arranged to sink heat away from the semiconductor device.

In this way an electronic package assembly is provided which has improved integration and good thermal management.

Brief Description of the Drawings

An exemplary embodiment of the invention will now be described with reference to the drawing in which:

FIG. 1 shows a preferred embodiment of an electronic package assembly in accordance with the invention;

FIG. 2 shows a block schematic diagram of the assembly of FIG. 1;

FIG. 3 shows an alternative embodiment of an electronic package assembly in accordance with the invention;

FIG. 4 shows a block schematic diagram of the assembly of FIG. 3;

FIG. 5 shows a top and a side view of an exemplary leadframe forming part of the assembly of FIG. 1 or FIG. 3;

FIG. 5a shows an alternative embodiment of the side view of FIG. 5; and,

FIG. 6 shows a top and a side view of an alternative exemplary leadframe forming part of the assembly of FIG. 1 or FIG. 3.

Detailed Description of a Preferred Embodiment

Referring to FIG. 1, there is shown an electronic package assembly 5 comprising double-sided leadless components (10, 14, 20) a printed circuit substrate 30, a leadframe comprising first (50) second (51) and third (52) elements and other electronic components (60, 70).

The substrate 30 is a multi-layered substrate of dielectric material and has top and bottom faces. The top face has a first set of printed circuit patterns 31-39, which facilitate connection of the substrate 30 to the double-sided leadless components (10, 14, 20) and also to the selected elements of the leadframe (50 and 52) to be further described below.

The substrate 30 also has a second set of printed circuit patterns 40-42 on the bottom face thereof. These second patterns 40-42 facilitate connection of the substrate 30 to the other electronic components (60, 70) which may be single or multiple packaged components. The first component 60 may be a packaged integrated circuit having electrical terminals 61 and 62 in the form of leads, and the second component 70 may be discrete device having electrical terminals 71 and 72 in the form of edge connectors.

The substrate also has a number of conductive vertical vias (43-47) which provide electrical and thermal paths between the top and the bottom faces of the substrate 30.

The double-sided leadless components (10, 14, 20) comprise first 10 and second 14 power switching transistors and an integrated circuit 20.
The first power switching transistor 10 may be a metal-oxide field effect transistor (MOSFET) or a bipolar transistor, and has a first electrode 11 (drain electrode) in the form of a pad located on an upper face and second and third electrodes 12 and 13 (source and gate electrodes respectively) in the form of pads located on a lower face. The second and third electrodes 12 and 13 form pads which are bonded via flip-chip solder bumps (of low thermal and electrical resistivity) to the printed circuit patterns 34 and 35 respectively of the substrate 30.

The second power switching transistor 14, which may also be a MOSFET or a bipolar transistor, has a first electrode 15 (drain electrode) in the form of a pad located on an upper face and second and third electrodes 16 and 17 (source and gate electrodes respectively) in the form of pads located on a lower face. The second and third electrodes 16 and 17 are bonded to the printed circuit patterns 33 and 32 respectively of the substrate 30.

In this way the first and second power switching transistors 10 and 14 respectively have vertical current paths between the upper and the lower faces (between drain and source electrodes).

The integrated circuit 20 may contain logic circuitry or similar, and has a lower face with pads 21 to 26 which are bonded to the printed circuit patterns 35, 32, 36 to 39 respectively. An optional further pad 27 may be provided on an upper face, to be further described below.

The leadframe is a plurality of unsupported (i.e. non-substrate supported) metal leads, including first (50) second (51) and third (52) elements. The first element 50 connects the printed circuit pattern 33 to the pad of the drain electrode 11 of the first power switching transistor 10 via bonds at both ends. Since the first element 50 does not form an external pin connection, it is regarded as an 'island' portion of the leadframe. The second element 51 has a first arm bonded to the further pad 27 of the integrated circuit 20, and a second arm bonded to the pad forming the drain electrode 15 of the second power switching transistor 14. The first and second arms of the second element 51 are connected in a section of the assembly 5 which is not shown. The third element 52 is bonded to the printed circuit pattern 31 of the substrate 30. The second element 51 and the third element 52 of the leadframe form power supply and ground terminals respectively (via external pins, not shown) and they are regarded as 'lead' portions.

Further circuit elements may be provided which are directly bonded to the leadframe. An example is shown in the form of component 80, which is attached between the first element 50 and the second element 51 of the leadframe 30.

Referring now also to FIG. 2, there is shown a block schematic diagram of the electronic package assembly 5, where each element of FIG. 2 has the same number as the corresponding of the assembly 5 of FIG. 1, with the exception of leads 63, 64 and 65, (which occupy a different plane of assembly 5 from that shown in FIG. 1) and component 80, which is exemplary only in FIG. 1 and therefore not shown in FIG. 2.

The integrated circuit 20, (which may be bare die, as illustrated) has various connections formed by the pads 21 to 26 and printed circuit patterns 35, 32, 36 to 39. In particular the printed circuit patterns 35 and 32 connect the integrated circuit 20 to the first and second power switching transistors 10 and 14 respectively.

Similarly the electronic component 60 (which may be a packaged integrated circuit, as illustrated) has various connections formed by the leads 61 to 65.

FIG. 2 also shows further optional power transistor stages (or branches) which could easily be formed in the assembly 5.

The first (drain) electrodes 11 and 15 of the first and second power switching transistors 10 and 14 respectively and those of the further optional power transistor stages, are

arranged to convey a large amount of current during operation, and the leadframe to which they are attached is specifically arranged to provide high current capacity.

In this way the PCB 30 provides logic interconnects for the assembly 5, and the leadframe provides power interconnects as well as external connections.

Referring now also to FIG. 3 and FIG. 4, there is shown an alternative arrangement of the assembly 5, having the same components with the same reference numerals. In this alternative arrangement, the first element 50 of the leadframe 30 is not arranged to connect the printed circuit pattern 33 to the drain electrode (pad 11) of the first power switching transistor 10. In this way a high-sided switch is formed instead of a bridge.

Referring now also to FIG. 5, there is shown a top view and a side view of a physical leadframe arrangement 100, having a substrate 130, on which a double-sided leadless semiconductor device 110 is mounted. Pads 112 and 113 of the semiconductor device 110, which are only shown in the top view, connect the semiconductor device 110 to 'island' portions 152 and 153 respectively of a leadframe. A further portion 157 of the leadframe, which is integral to portions 152 and 153, provides a vertical connection to the substrate 130. A stub portion 158 provides yet another connection of the leadframe, which may be to a further device, a further substrate, or to the substrate 130.

In an alternative embodiment illustrated in FIG. 5a, the further portion 157 of the substrate is replaced by a solder ball 159, which provides a connection to the substrate 130.

A further double-sided leadless semiconductor device 120 is also mounted on the substrate 130. Pads 114 and 115 of the semiconductor device 120, which are only shown in the top view, connect the semiconductor device 120 to portions 154 and 155 respectively of the leadframe. The portions 154 and 155 have pin protrusions which extend beyond an encapsulation 140 (shown by the dashed line of the side view), such that the pin protrusions provide external connections for the devices 110 and 120.

Referring now also to FIG. 6, there is shown an alternative leadframe arrangement 200, which is identical to the arrangement 100 of FIG. 5 except that the leadframe portions 154 and 155 have been replaced with raised leadframe pads 164 and 165. These pads 164 and 165 extend beyond the encapsulation 140, as shown by the dashed line of the side

view, and hence provide an alternative form of external connection for the devices 110 and 120.

It will be appreciated that further alternative embodiments to those described above are possible. For example, it is envisaged that two or more printed circuit substrates could be incorporated into the assembly 5, using flip-chip techniques with double-sided components to replace the components 60 and 70.

Furthermore other combinations of interconnections and leads of the leadframes shown above are possible.

Claims

1. An electronic package assembly, comprising:

a plurality of semiconductor devices, each having a first side with a plurality of conductive pads, at least two of the plurality of devices being vertical power transistor devices having a second side opposite the first side, the second side having further conductive pads;

a printed circuit substrate, having a plurality of printed circuit patterns bonded to the conductive pads of the first sides of the plurality of semiconductor devices, and arranged to provide logic interconnections between the plurality of semiconductor devices; and,

a leadframe including leads which provide external connections for the package assembly, and having a non-lead island portion bonded to the further conductive pads of the second sides of the at least two vertical power transistor devices,

wherein the island portion of the leadframe forms a power interconnection between the at least two vertical power transistor devices.

2. The assembly of claim 1 wherein the leadframe further comprises a substrate lead portion, which is arranged to connect to a further pad of the printed circuit substrate, thereby directly connecting the leadframe to the substrate.

3. The assembly of claim 2 wherein the substrate lead portion is connected to the island portion of the leadframe such that the conductive pads of the second sides of the semiconductor devices are directly electrically connected to the substrate.

4. The assembly of claim 1 wherein a discrete electronic device is mounted directly onto the leadframe.

5. The assembly of claim 4 wherein the leadframe has contact bumps to which the electronic device is coupled.

6. The assembly of any preceding claim wherein the at least two semiconductor devices form a vertical H-bridge power transistor arrangement.

7. The assembly of any preceding claim the at least two semiconductor devices form a full-bridge high-sided switch arrangement.

8. The assembly of any preceding claim wherein the substrate has a first face having the plurality of pads, and a second face opposite the first face to which further electronic devices are attached.

9. The assembly of claim 8 wherein the substrate is provided with electrical vias arranged to electrically interconnect the first and the second faces of the substrate.

10. The assembly of any preceding claim wherein the substrate is provided with thermal vias arranged to sink heat away from the semiconductor device.

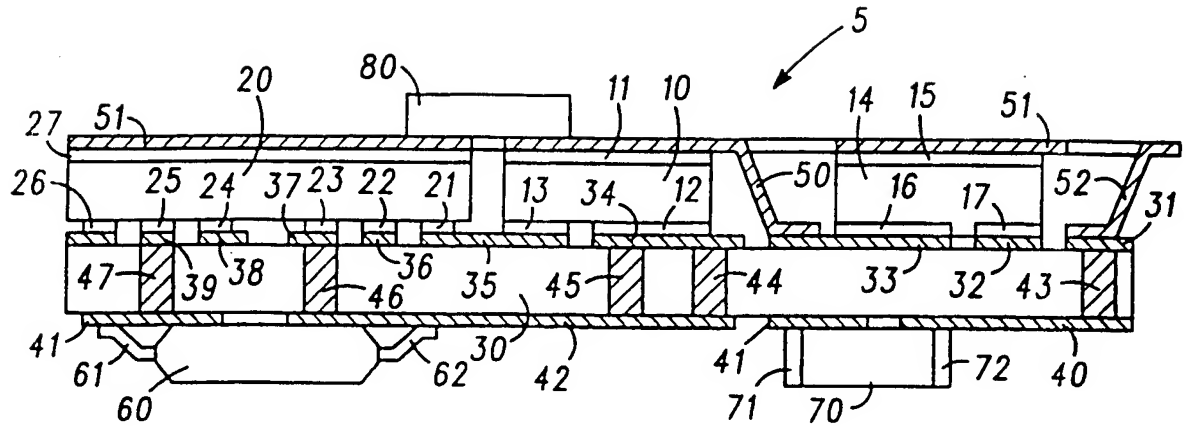


FIG. 1

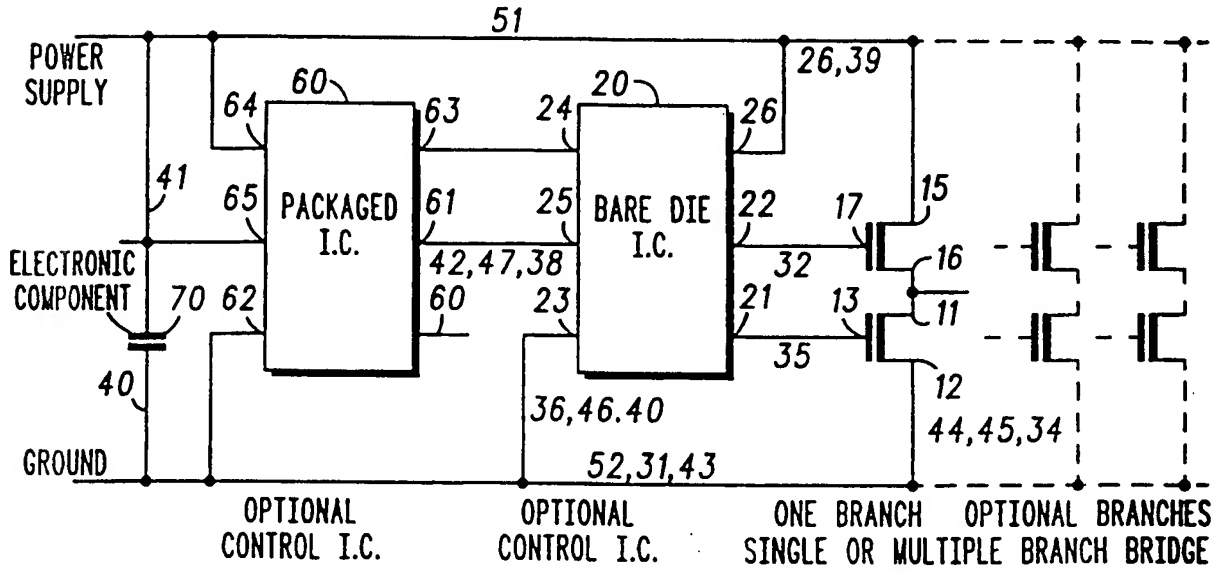


FIG. 2

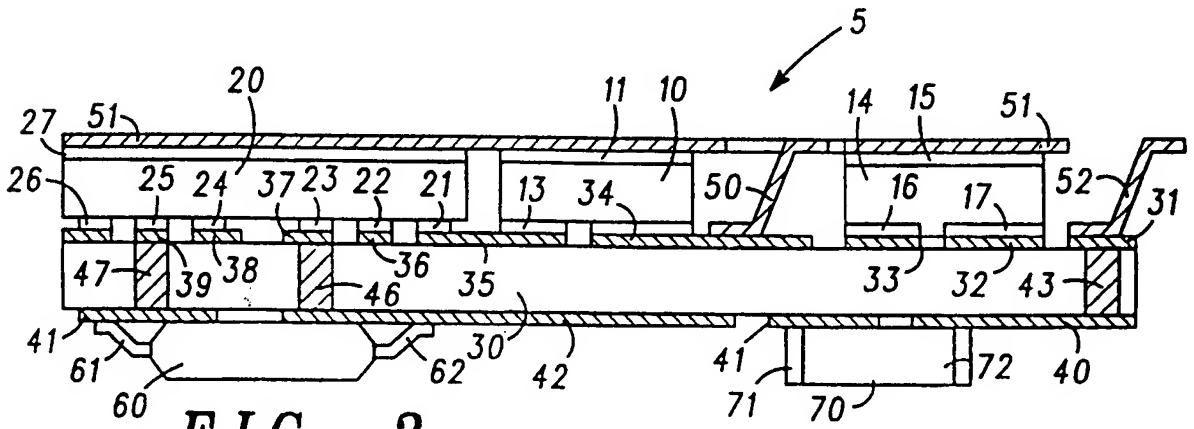


FIG. 3

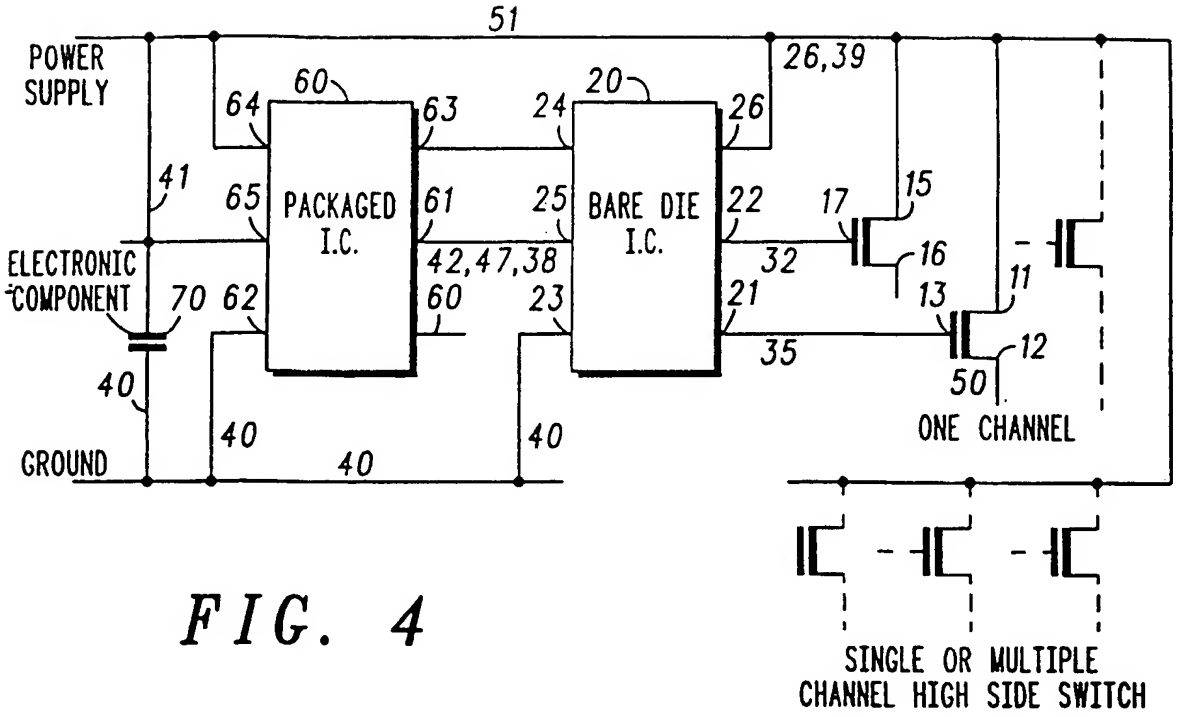


FIG. 4

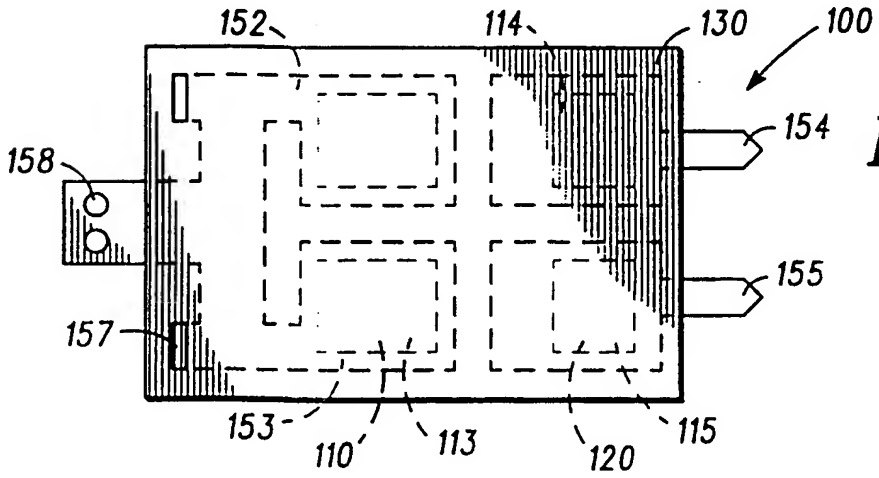


FIG. 5

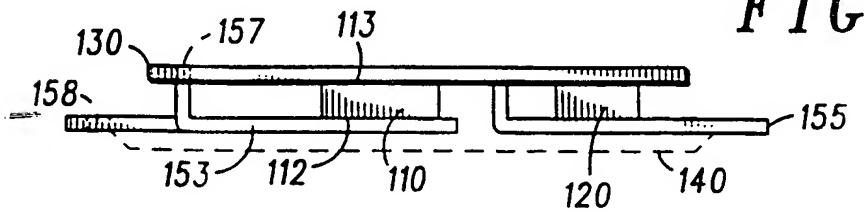


FIG. 5B

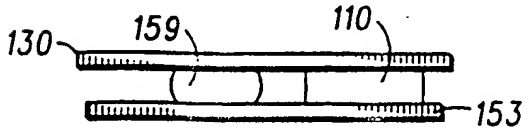


FIG. 5A

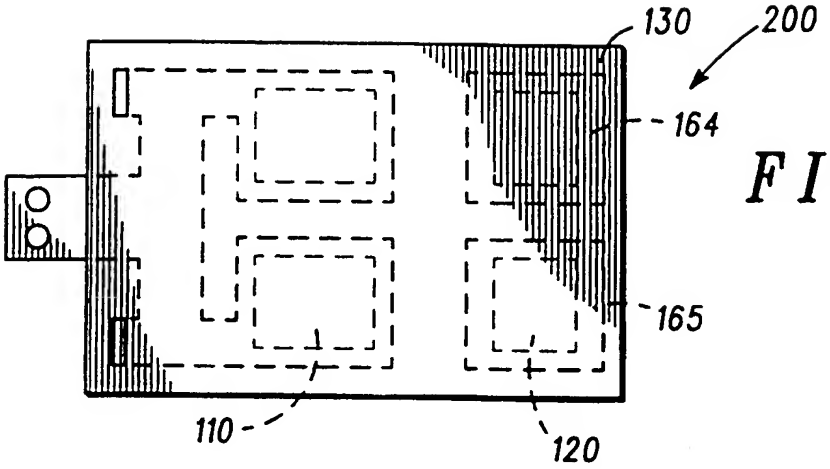


FIG. 6

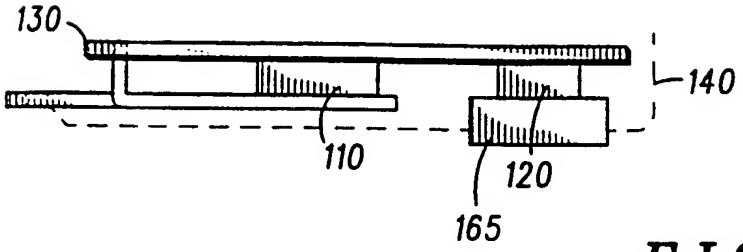


FIG. 6A